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(54) Correction of D.C. offset in received and demodulated radio signals.

(57) A received and demodulated multi-level signal (32) is corrected for D.C. offset by means of a feedback loop (34) which applies a correction signal (38) to the multi-level signal (32). Initial coarse correction is provided by feeding the corrected signal (42) into the feedback loop where a low pass filter (36) averages the corrected signal over time and detects departure from zero of this time-averaged signal. After initial coarse correction, finer correction of D.C. offset is provided in a data-aided mode in which detected data values (46) are fed into the feedback loop (34). The method achieves D.C. offset correction without the need to know anything about the data pattern of the received signal (32).

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Field of the Invention

This invention relates to a method of and apparatus for correcting D.C. offset in a multi-level digital signal which has been received and demodulated in a radio. The invention is particularly, but not exclusively, applicable to the correction of D.C. offset in the multi-level digital signal emanating from a frequency discriminator, prior to signal detection.

Background to the Invention

For digital frequency modulated (or phase modulated) systems employing frequency discriminator receivers, the output circuit of the discriminator needs to be D.C. coupled since the demodulated baseband signal contains a D.C. component. Any frequency error in the frequency modulated carrier before a frequency discriminator receiver appears as an additional D.C. offset in the discriminator output signal, so that all the received data symbols are offset from their nominal voltage levels by a fixed amount that is directly proportional to the frequency error. This offset, if not compensated correctly before going through the threshold level detection, causes an increase in detection error and hence performance degradation. In the worst case, the D.C. offset is so large that the received data symbols fall into incorrect detection bands, leading to erroneous detection even in the absence of noise. Although the receiver normally employs automatic frequency control (AFC) to track the carrier frequency, it often adapts too slowly and even a residual frequency error of several hundred Hertz may be sufficient to cause noticeable increase in detection error. Furthermore, the practical analogue frequency discriminator circuit itself may often contain some imbalance, causing further D.C. offset in its output signal. This offset varies from component to component and drifts with temperature. To reduce or compensate it using conventional analogue methods increases circuit complexity and receiver costs.

Prior Art

US Patent 4873702 (Chiu) discloses a method of correcting D.C. offset in multilevel digitally modulated signals. The data transmission system of Chiu is arranged to send a particular preamble signal each time a different data source begins transmission of its data. The present invention aims to provide a method of and apparatus for correction of D.C. offset not requiring the transmission of any particular preamble signal.

Summary of the Invention

According to one aspect the invention provides a method of correcting D.C. offset in a multi-level digital signal which has been received and demodulated, comprising employing a feedback loop to generate a correction signal which is fed back and applied to the uncorrected signal so as to correct the latter without the need for any knowledge about the data pattern of the received signal, wherein the method includes coarse correction, during which comparatively large D.C. offsets can be tolerated followed by fine correction, during which comparatively small D.C. offsets only can be tolerated.

The invention thus has the advantage that it is compatible with digital cellular radio communications systems currently being adopted by national and intra-national standards-setting authorities, in which the transmitted data does not incorporate a preamble, or other component, included specially for D.C. offset correction purposes.

Preferably, the corrected signal is averaged over time in the feedback loop and the correction signal is representative of the departure from zero of the time-averaged corrected signal. The feedback loop may include a low pass filter which averages the corrected signal over time and which produces the correction signal.

In the preferred embodiment the multi-level signal, after detection, is applied to the feedback loop, the correction signal being representative of the detected signal. The detected signal is conveniently subtracted from the corrected signal and the resultant difference signal is averaged over time in the low pass filter, the output of which provides the correction signal.

The multi-level signal may be derived from a digital frequency discriminator in system hardware, or in an alternative arrangement the multi-level signal can be derived from an analogue frequency discriminator, the output of which is passed through an analogue to digital convertor before application of the inventive correction method.

According to another aspect the invention provides apparatus for correcting D.C. offset in a multi-level digital signal which has been received and demodulated, the apparatus comprising a feedback loop operative to generate a correction signal which is fed back and applied to the uncorrected signal so as to correct the latter without the need for any knowledge about the data pattern of the received signal, means for injecting into the loop non data-aided correction values in order to implement coarse correction during which comparatively large D.C. offsets can be tolerated, and means for injecting into the loop data-aided correction values in order to implement fine correction during which comparatively small D.C. offsets only can be tolerated.

Brief Description of the Drawings

The invention will now be further described, by

way of example, with reference to the accompanying drawings, in which:

Figure 1 shows in block diagrammatic form a demodulator which employs digital frequency discrimination and which produces a multi-level output signal suitable for correction by the invention,

Figure 2 shows in block diagrammatic form a demodulator similar to that of Figure 1 but employing analogue frequency discrimination,

Figure 3 explains the nature of the multi-level digital output signal produced by the demodulator of Figure 1 or Figure 2, and

Figure 4 shows in block diagrammatic form a circuit according to the invention and for correcting D.C. offset in the multi-level output signal of the demodulator of Figure 1 or Figure 2.

Description of Preferred Embodiments

The demodulator of Figure 1 is intended to be included in the receiver section of a hand-held mobile radio. The transmitted signal consists of a sinusoidal carrier modulated by differential quaternary phase shift keying (DQPSK) to carry the transmitted information. The carrier is converted to a fixed intermediate frequency of 450 KHz, in accordance with conventional practice, to provide an intermediate frequency (IF) signal indicated at 10 in Figure 1.

The signal 10 is fed to a limiter amplifier 12 which transforms the signal 10 to a rectangular output waveform 14 by taking a narrow slice of a signal about the value zero and amplifying the sliced signal to the required level. The variations in the phase of the signal 10 are thus preserved in the signal 14.

The signal 10 is generally sinusoidal but in each symbol period T the phase of the carrier is varied or modulated to code a transmitted symbol value. The modulation is to level four, meaning that in each symbol period, the phase is modulated to any one of four different levels. This four level modulation enables two bits of binary information to be coded by each phase shift, thus:

- Phase shifted by $+\frac{\pi}{4}$ radians means 00 bit pair (or symbol value +1)
- Phase shifted by $+\frac{3\pi}{4}$ radians means 01 bit pair (or symbol value +3)
- Phase shifted by $-\frac{\pi}{4}$ radians means 10 bit pair (or symbol value -1)
- Phase shifted by $-\frac{3\pi}{4}$ radians means 11 bit pair (or symbol value -3)

Hence, the phase shift of the signal 10 in each symbol period T is representative of the transmitted bit pair of that symbol. The phase of the carrier does not alter suddenly at a symbol period transition. There is a progressive alteration in phase throughout the symbol period, the fastest change in phase occuring in the central region of the symbol period T.

The system digital hardware (called ASIC) 16 receives the signal 14 and, by frequency discrimination, derives an output signal S(i) which, for each symbol period T, is at one of four levels depending on the phase of modulation. This derivation is explained in greater detail in the applicants' co-pending UK Patent Application No 9223931.8.

Figure 2 shows an alternative demodulator using analogue frequency descrimination. Referring to Figure 2, an intermediate frequency signal 20 (which consists of a sinusoidal carrier modulated by DQPSK so as to carry transmitted symbol values) is fed to a limiter amplifier 22 and thence to an analogue frequency discriminator 23 having a delay line 24 and a low pass filter 25. The discriminator 23 produces a frequency deviation signal which needs to be integrated over each symbol period to derive an output signal representative of the carrier phase change and, therefore, the transmitted signal. The output of the analogue frequency discriminator 23 is converted to digital format in an analogue to digital converter 26 and then fed to digital hardware 27, in which the signal is integrated and dumped into one of four decision bands depending on the modulation phase which is representative of the transmitted symbol value. The hardware 27 produces an output signal S(i).

Figure 3 explains the nature of the signal S(i) produced by the demodulator of Figure 1 or Figure 2.

Ideally, if the phase shift in any symbol period T is $\frac{\pi}{4}$, the output signal S(i) will be at a level representative of +1, indicating that the bit pair for that symbol is 00; similarly:

- An S(i) level of +3 indicates a phase shift of $\frac{3\pi}{4}$, indicating the bit pair 01
- An S(i) level of -1 indicates a phase shift of $-\frac{\pi}{4}$, indicating the bit pair 10
- An S(i) level of -3 indicates a phase shift of $-\frac{3\pi}{4}$, indicating the bit pair 11.

In practice, the signal level S(i) will not be exactly 0, +1, +3, -1 or -3 and there will be a band of signal levels, centred on each ideal level. For example, if the signal level S(i) falls within the signal band 30 centred on +1, a subsequent decision will be made to ascribe level +1 to that signal. It will be appreciated that the other signal levels have corresponding decision bands, each centred on the corresponding level.

As previously mentioned, any D.C. error in the signal S(i) impairs performance and may cause the signal level to fall in an incorrect detection band, leading to erroneous detection. For example, if there is a D.C. offset which lifts all the signals by a value of plus

1 in Figure 3, a signal which would be near the top of the decision band 30 in the absence of the offset would be taken into the decision band centered on plus 3, and incorrect detection would therefore ensue. The invention aims to correct such D.C. offset which in the digital case of Figure 1 can arise from frequency error or from errors in the data itself, and in the analogue case of Figure 2 can arise from these two causes, plus the further possible cause of analogue circuit variations, eg drift with temperature.

D.C. offset in the signal S(i) is corrected by the circuit shown diagrammatically in Figure 4. The signal S(i) is applied at input 32. A recursive feedback loop 34, incorporating a low pass filter 36, produces a correction signal 38 which is subtracted from S(i) in algebraic summer 40 to produce a corrected signal 42.

The corrected signal 42 is fed to a detector 44 which places the corrected signal S(i) into one of the decision bands. For example, if the corrected S(i) for a particular symbol period falls within decision band 30 (Figure 3) the detector 44 ascribes a phase value of$_4$ to that particular symbol period. Hence, the output 46 of the detector 44 is a stream of phase values, corresponding to the sequence of phase modulation imparted to the signal received by the demodulator of Figure 1 or Figure 2.

During initial synchronisation, coarse correction is achieved by the feedback loop which takes the signal 42, averages it over time (eg half second) in the filter 36 and produces a correction signal 38 which is representative of the departure from zero of the time-averaged signal 42. This non data-aided correction relies on the fact that over time the average of the multi-level signal 32 will be zero. No knowledge about the data pattern of the received signal is necessary, in contrast to the prior art which relies on a known preamble signal. Hence, correct detection of data symbols takes place in the presence of large D.C. offset errors, resulting from large frequency errors. This is the non data-aided option indicated at 48 in Figure 4.

After initial synchronisation, the data-aided option, indicated at 50, is implemented, providing finer correction. In this mode, the detected value signal 46 is applied as an input to the feedback loop 34. The signal 46 is subtracted from signal 42 in an algebraic summer 52, the resultant error signal 54 being averaged over time in the low pass filter 36 which produces the correction signal 38. The data-aided feedback loop can only tolerate moderate amounts of D.C. offset and acts to correct any biasing in the data pattern itself, for example if on average there are more positive data symbols than negative ones, this would cause a small D.C. offset in S(i). The data-aided recursive loop will also provide a continuous tracking of any variation of D.C. offset in the analogue circuit of Figure 2. Here again, D.C. offset correction is achieved without the need for a preamble signal.

In the case of a modulator using digital frequency discrimination (eg Figure 1) the correction circuit of Figure 4 preferably has a second recursive feedback loop 56 for providing automatic frequency tuning. This second feedback loop has an algebraic summer 58 which derives a correction signal 60 from the difference between signals 32 and 46. The correction signal 60 is fed to a low pass filter 62 which averages the signal 60 over time and produces a digital correction signal 64. This is fed through a digital to analogue convertor (not shown) which then drives the frequency controller of the voltage controlled crystal oscillator which in turn controls the frequency of the input signal.

Claims

1. A method of correcting D.C. offset in a multi-level digital signal which has been received and demodulated, comprising employing a feedback loop (34) to generate a correction signal (38) which is fed back and applied to the uncorrected signal so as to correct the latter without the need for any knowledge about the data pattern of the received signal, characterised in that the method includes coarse correction, during which comparatively large D.C. offsets can be tolerated followed by fine correction, during which comparatively small D.C. offsets only can be tolerated.

2. A method according to claim 1, characterised in that during said coarse correction the corrected signal is averaged over time in the feedback loop (34) and the correction signal (38) is representative of the departure from zero of the time-averaged corrected signal.

3. A method according to claim 2, characterised in that the feedback loop (34) includes a low pass filter (36) which averages the corrected signal over time and which produces the correction signal (38).

4. A method according to any of the preceding claims, characterised in that during said fine correction the multi-level signal, after detection, is applied to the feedback loop (34), the correction signal (38) being representative of the detected signal.

5. A method according to claim 4, characterised in that the detected signal is subtracted from the corrected signal and the resultant difference signal is averaged over time in a low pass filter (62), the output of which provides the correction signal (64).

6. A method according to any of the preceding

claims characterised in that the multi-level signal, after detection, is applied to an automatic frequency control circuit.

7. A method according to any of the preceding claims, characterised in that the multi-level signal is derived from a digital frequency discriminator in system hardware.

8. A method according to any of claims 1 to 6, characterised in that the multi-level signal is derived from an analogue frequency discriminator, the output of which is passed through an analogue to digital convertor before D.C. correction.

9. Apparatus for correcting D.C. offset in a multi-level digital signal which has been received and demodulated, the apparatus comprising a feedback loop (34) operative to generate a correction signal (38) which is fed back and applied to the uncorrected signal so as to correct the latter without the need for any knowledge about the data pattern of the received signal, characterised by means (48) for injecting into the loop (34) non data-aided correction values in order to implement coarse correction during which comparatively large D.C. offsets can be tolerated, and means (50) for injecting into the loop (34) data-aided correction values in order to implement fine correction during which comparatively small D.C. offsets only can be tolerated.

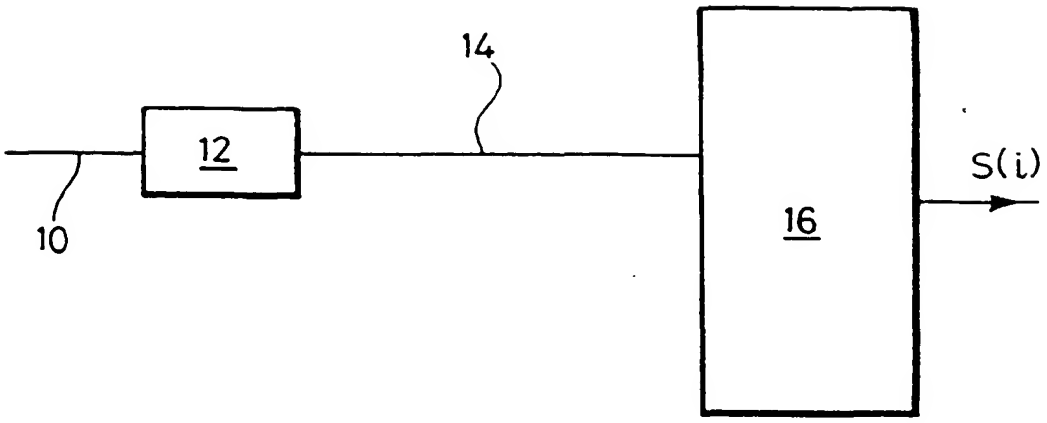

Fig. 1

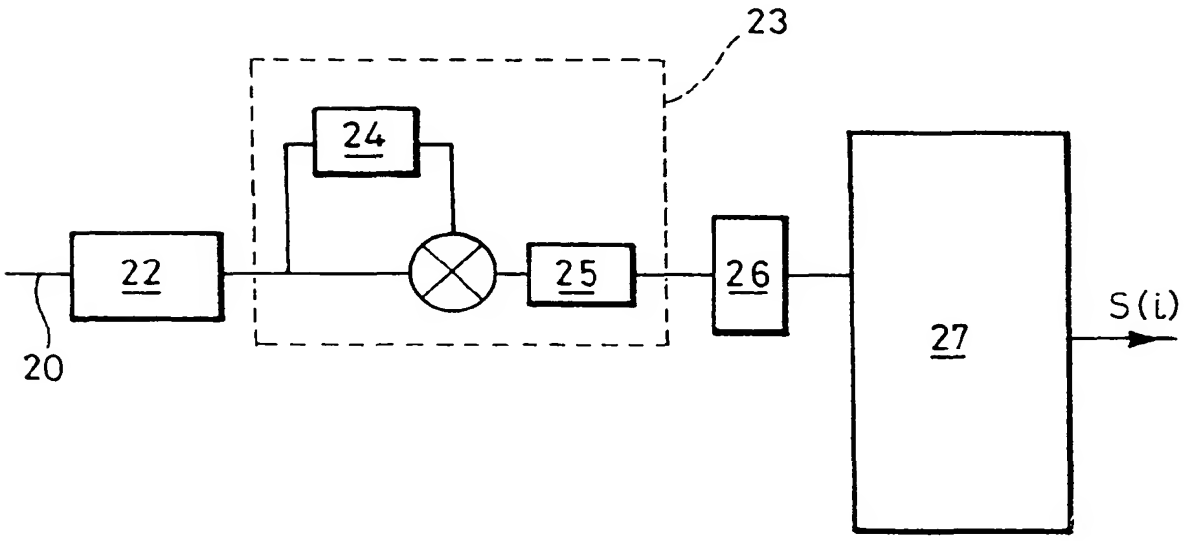

Fig. 2

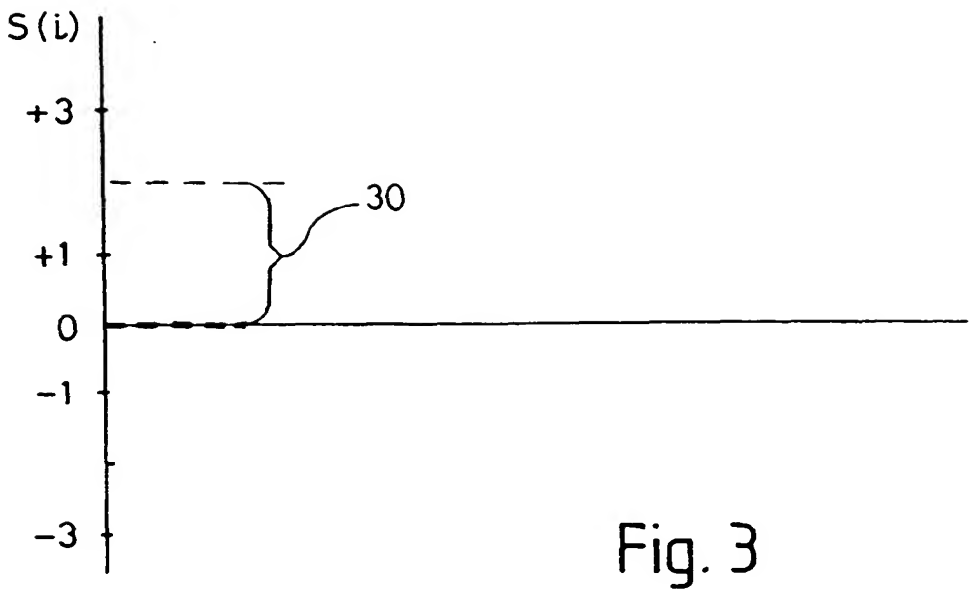

Fig. 3

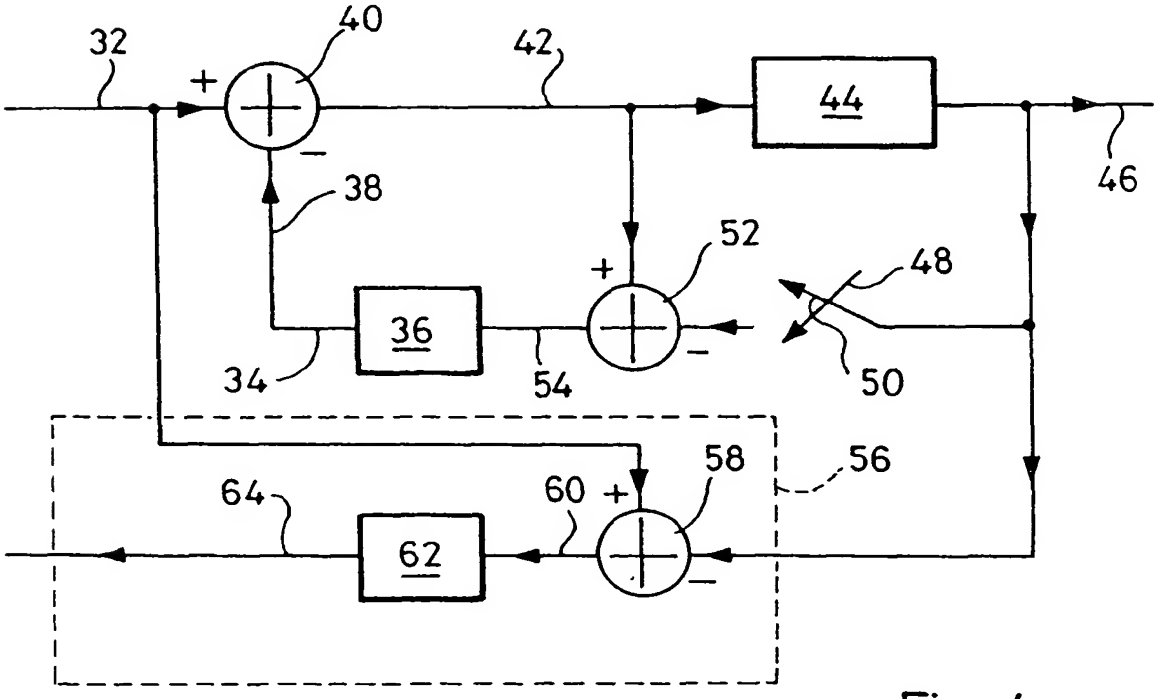

Fig. 4

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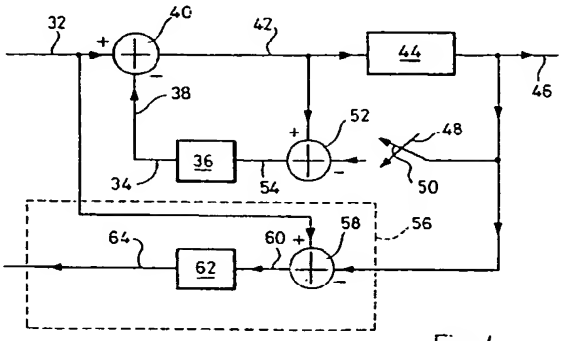

Fig. 4

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EUROPEAN SEARCH REPORT

Application Number EP 94300483.8

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP - A - 0 153 708 (NIPPON TELEGRAPH AND TELEPHONE PUBLIC CORPORATION) * Totality * --	1,9	H 04 L 27/38 H 04 L 25/06
A	EP - A - 0 254 877 (FUJITSU LIMITED) * Totality * --	1,9	
A	WO - A - 92/13 415 (MOTOROLA INC.) * Description * --	1,9	
A	US - A - 4 553 102 (YAS UHARU YOSHIDA) * Description; column 2, lines 22-41 * --	1,9	
A	US - A - 4 250 458 (R.L. RICHMOND, P.F. WYAR) * Description; column 3, line 30 - column 4, line 16 * --	1,9	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H 03 D 1/00 H 04 L 25/00 H 04 L 27/00
A	GB - A - 1 451 546 (SIEMENS) * Description * --	1,9	
D,A	US - A - 4 873 702 (RAN-FUN CHIU) ----		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	28-04-1995	ZUGAREK

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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